Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method in a data processing system for monitoring processing of instructions, the method comprising:

receiving, from an instruction storage area storing instructions, an instruction at a processor for execution;

responsive to a determination of being in an enabled state to perform a selected action, determining whether the instruction is associated with [[an]] a performance indicator stored in a shadow memory, the shadow memory comprising a storage area separate from [[an]] the instruction storage area ~~in which the instruction is stored~~ and storing performance indicators associated with instructions stored in the instruction storage area; and

performing the selected action ~~in response to the~~ if a performance indicator ~~being~~ is associated with the instruction.

2. (Currently amended) The method of claim 1, ~~wherein the instruction is received in an instruction cache and~~ further comprising:

executing the instruction after receiving the instruction for execution.

3. (Previously presented) The method of claim 1, wherein the determination of being in an enabled state comprises:

examining a register in the processor; and

determining whether the register is set to indicate the enabled state.

4. (Original) The method of claim 1, wherein the selected action includes at least one of sending the instruction to a performance monitor unit, sending the instruction to a data cache, and sending the instruction to an interrupt unit.

5. (Original) The method of claim 1, wherein the instruction is received in a bundle.

6. (Original) The method of claim 1, wherein the enabled state is enabled by setting a register in a processor.

7. (Original) The method of claim 1, wherein the shadow memory contains debugging information.

8. (Currently amended) A method in a data processing system for monitoring access to data during execution of instructions by a processor, the method comprising:

responsive to a determination of being in an enabled state to perform a selected action when a data access to a memory location occurs, determining whether the memory location is associated with [[an]] a performance indicator stored in a shadow memory, the shadow memory comprising a storage area separate from ~~the~~ memory ~~location~~ locations in which data is stored and storing performance indicators associated with memory locations in which data is stored; and

performing the selected action ~~in response to the~~ if a performance indicator ~~being~~ is associated with the memory location.

9. (Previously presented) The method of claim 8, wherein the selected action is at least one of forcing an interrupt and counting accesses to the memory location.

10. (Original) The method of claim 8, wherein the shadow memory includes a shadow word for each word of data.

11. (Previously presented) The method of claim 8, wherein the determination of being in an enabled state comprises:

examining a register in the processor; and

determining whether the register is set to indicate the enabled state.

12. (Currently amended) A data processing system for monitoring processing of instructions, the data processing system comprising:

receiving means for receiving, from an instruction storage area storing instructions, an instruction at a processor for execution;

determining means, responsive to a determination of being in an enabled state to perform a selected action, for determining whether the instruction is associated with [[an]] a performance indicator stored in a shadow memory, the shadow memory comprising a storage area separate from [[an]] the instruction storage area and storing performance indicators which are associated with instructions stored in the instruction storage area ~~in which the instruction is stored~~; and

performing means for performing the selected action ~~in response to~~ if a [[the]] performance indicator ~~being~~ is associated with the instruction.

13. (Previously presented) The data processing system of claim 12, wherein the determining means is a first determining means and further comprising:

examining means for examining a register in the processor; and

second determining means for determining whether the register is set to indicate the enabled state.

14. (Original) The data processing system of claim 12, wherein the selected action includes at least one of sending the instruction to a performance monitor unit, sending the instruction to a data cache, and sending the instruction to an interrupt unit.

15. (Original) The data processing system of claim 12, wherein the instruction is received in a bundle.

16. (Currently amended) A data processing system for monitoring access to data during execution of instructions by a processor, the data processing system comprising:

determining means, responsive to a determination of being in an enabled state to perform a selected action when a data access to a memory location occurs, for determining whether the memory location is associated with an indicator stored in a shadow memory, the shadow memory comprising a storage area separate from [[the]] memory ~~location~~ locations in which data is stored, and storing performance indicators associated with memory locations in which data is stored; and

performing means for performing the selected action ~~in response to~~ if a performance [[the]] indicator ~~being~~ is associated with the memory location.

17. (Previously presented) The data processing system of claim 16, wherein the selected action is at least one of forcing an interrupt and counting accesses to the memory location.

18. (Original) The data processing system of claim 16, wherein the shadow memory includes a shadow word for each word of data.

19. (Currently amended) A computer program product in a computer readable recordable-type medium for monitoring processing of instructions, the computer program product comprising:

first instructions for receiving, from an instruction storage area storing instructions, an instruction at a processor for execution;

second instructions, responsive to a determination of being in an enabled state to perform a selected action, for determining whether the instruction is associated with an indicator stored in a shadow memory, the shadow memory comprising a storage area separate from [[an]] the instruction storage area and storing performance indicators associated with instructions stored in the instruction storage area ~~in which the instruction is stored~~; and

third instructions for performing the selected action ~~in response to~~ if a performance [[the]] indicator ~~being~~ is associated with the instruction.

20. (Previously presented) The computer program product of claim 19, wherein the second instructions comprise:

first sub-instructions for examining a register in the processor; and

second sub-instructions for determining whether the register is set to indicate the enabled state.

21. (Original) The computer program product of claim 19, wherein the selected action includes at least one of sending the instruction to a performance monitor unit, sending the instruction to a data cache, and sending the instruction to an interrupt unit.

22. (Original) The computer program product of claim 19, wherein the instruction is received in a bundle.

23. (Currently amended) A computer program product in a computer readable recordable-type medium for monitoring access to data during execution of instructions by a processor, the computer program product comprising:

first instructions, responsive to a determination of being in an enabled state to perform a selected action when a data access to a memory location occurs, for determining whether the memory location is associated with [[an]] a performance indicator stored in a shadow memory, the shadow memory comprising a storage area separate from [[the]] memory ~~location~~ locations in which [[the]] data is stored and storing performance indicators associated with memory locations in which data is stored; and

second instructions for performing the selected action ~~in response to~~ if a performance [[the]] indicator ~~being~~ is associated with the memory location.

24. (Previously presented) The computer program product of claim 23, wherein the selected action is at least one of forcing an interrupt and counting accesses to the memory location.

25. (Original) The computer program product of claim 23, wherein the shadow memory includes a shadow word for each word of data.